IN THE CLAIMS

1. Claims 18-24, 26-39 and 41-48 are now pending in the application as follows:

[1. An impedance blocking filter circuit used in telecommunication systems for interconnecting between incoming telephone lines and customer's terminal equipment so as to unconditionally block impedances from above 20 KHz due to the customer's terminal equipment from an ADSL network unit and/or home networking interface unit, said filter circuit comprising:

first and second third inductors connected in series between a first input terminal and a first common point;

said first inductor having its one end connected to said first input terminal and its other end connected to one end of said second inductor, said second inductor having its other end connected to said first common point;

third and fourth inductors connected in series between a second input terminal and a second common point;

said third inductor having its one end connected to said second input terminal and its other end connected to one end of said fourth inductor, said fourth inductor having its other end connected to said second common point;

first switching means having a first end and a second end and being responsive to DC loop current for electrically connecting said first end to said second end;

a first capacitor having a first end connected to said first common point and a second end connected to said first end of said switching means, said second end of said switching means being connected to said second common point;

a fifth inductor having a first end connected to said first common point and a second end connected to a first output terminal, and a sixth inductor having a first end connected to said second common point and a second end connected to a second output terminal;

second switching means having a first end and a second end and being responsive to said DC loop current for electrically connecting said first end to said second end;

a second capacitor having a first end connected to said sixth inductor at a first node and a second end connected to said first end of said second switching means, said second end of said second switching means being connected to said fifth inductor at a second node;

switch suppression circuit means interconnected between said first and second common points for preventing transients caused by actuation of said first and second switching means from being fed back into the incoming telephone lines; and

correction circuit means interconnected between said first and second nodes and said output terminals for significantly reducing return loss caused by inductive impedance when the customer's terminal equipment goes off-hook.

2. An impedance blocking filter circuit as claimed in claim 1, wherein said correction circuit means is comprised of a first tank circuit and a second tank circuit, said first tank circuit being formed of a first winding inductor, a first tank capacitor, and a first tank resistor all connected in parallel and between said first node and said first output terminal, second tank circuit being formed of a second winding inductor, a second tank capacitor, and a second tank resistor all connected in parallel and between said second node and said second output terminal.

3. An impedance blocking filter circuit as claimed in claim 2, further comprising a seventh inductor having a first end connected to said fifth inductor at said first node and a second end connected to said first tank circuit, and an eighth inductor having a first end connected to said sixth inductor at said second node and a second end connected to said second tank circuit.

4. An impedance blocking filter circuit as claimed in claim 3, wherein said first switching means includes a first reed switch and said second switching means includes a second reed switch.

5. An impedance blocking filter circuit as claimed in claim 4, wherein said first winding of said first tank circuit, said second winding of said second tank circuit, said first reed switch, and said second reed switch are arranged in a dual winding inductor structure.

6. An impedance blocking filter circuit as claimed in claim 5, wherein said first winding of said first tank circuit and said first reed switch is arranged in a first current sensor unit, said second winding of said second tank circuit and said second reed switch is arranged in a second current sensor unit.

7. An impedance blocking filter circuit as claimed in claim 1, further comprising a first metal-oxide or silicon varistor connected in series with said first capacitor and in parallel with said first switching means, and a second metal-oxide or silicon varistor connected in series with said second capacitor and in parallel with said second switching means.

8. An impedance blocking filter circuit as claimed in claim 7, wherein said switch suppression circuit means includes a ninth inductor, a tenth inductor, and a third capacitor.

9. An impedance blocking filter circuit as claimed in claim 8, wherein said ninth inductor has a first end connected to said second inductor and a second end connected to said fifth inductor, said tenth inductor has a first end connected to said fourth inductor and a second end connected to said sixth inductor, and said third capacitor has a first end connected to the junction of said second and fifth inductors and a second end connected to the junction of said third and sixth inductors.

10. An impedance blocking filter circuit used in telecommunication systems for interconnecting between incoming telephone lines and customer's terminal equipment so as to unconditionally block impedances from above 20 KHz due to the customer's terminal equipment from an ADSL network unit and/or home networking interface unit, said filter circuit comprising:

first and second third inductors connected in series between a first input terminal and a first common point;

said first inductor having its one end connected to said first input terminal and its other end connected to one end of said second inductor, said second inductor having its other end connected to said first common point;

third and fourth inductors connected in series between a second input terminal and a second common point;

said third inductor having its one end connected to said second input terminal and its other end connected to one end of said fourth inductor, said fourth inductor having its other end connected to said second common point;

transistor switching means interconnected between said first and second common points and being responsive to DC loop current for eliminating shunt capacitance caused by other filter circuits connected to on-hook telephone sets;

a fifth inductor having a first end connected to said first common point and a second end connected to a first output terminal, and a sixth inductor having a first end connected to said second common point and a second end connected to a second output terminal; and

correction circuit means interconnected between said fifth and sixth inductors and said output terminals for significantly reducing return loss caused by inductive impedance when the customer's terminal equipment goes off-hook.

11. An impedance blocking filter circuit as claimed in claim 10, wherein said transistor switching means is comprised of a pair of transistors, a resistor, first and second capacitors, and first and second varistors.

12. An impedance blocking filter circuit as claimed in claim 10, wherein said correction circuit means is comprised of a first tank circuit and a second tank circuit, said first tank circuit being formed of a first winding inductor, a first tank capacitor, and a first tank resistor all connected in parallel and between said fifth inductor and said first output terminal, second tank circuit being formed of a second winding inductor, a second tank capacitor, and a second tank resistor all connected in parallel and between said sixth inductor and said second output terminal.

13. An impedance blocking filter circuit used in telecommunication systems for interconnecting between incoming telephone lines and customer's terminal equipment so as to unconditionally block impedances from above 20 KHz due to the customer's terminal equipment from an ADSL network unit and/or home networking interface unit, said filter circuit comprising:

first and second inductors connected in series between a first input terminal and a first common point;

said first inductor having its one end connected to said first input terminal and its other end connected to one end of said second inductor, said second inductor having its other end connected to said first common point;

third and fourth inductors connected in series between a second input terminal and a second common point;

said third inductor having its one end connected to said second input terminal and its other end connected to one end of said fourth inductor, said fourth inductor having its other end connected to said second common point;

first switching means having a first end and a second end and being responsive to DC loop current for electrically connecting said first end to said second end;

a first capacitor having a first end connected to said first common point and a second end connected to said first end of said switching means, said second end of said switching means being connected to said second common point; and

switch suppression circuit means interconnected between said first and second common points for preventing transients caused by actuation of said first switching means from being fed back into the incoming telephone lines.

14. An impedance blocking filter circuit as claimed in claim 13, further comprising a fifth inductor having a first end connected to said first common point and a second end connected to a first output terminal, and an sixth inductor having a first end connected to said second common point and a second end connected to a second output terminal.

15. An impedance blocking filter circuit as claimed in claim 14, wherein said first switching means includes a reed switch.

16. An impedance blocking filter circuit as claimed in claim 15, wherein said first through fourth inductors and said reed switch are arranged in a dual winding ferrite core inductor device.

17. An impedance blocking filter circuit as claimed in claim 13, further comprising a metal-oxide varistor connected in series with said first capacitor and in parallel with said first switching means.]

18. A telecommunication impedance blocking filter circuit, comprising:

at least one input terminal;

at least one output terminal;

a first filter stage disposed in electrical series between said at least one input and output terminals;

a second filter stage disposed in electrical series with said first filter stage, said second stage comprising a capacitor and switch disposed in series with at least one another;

a third filter stage disposed in electrical series with said second filter stage; and

a fourth filter stage disposed in electrical series with said third filter stage, said fourth stage being specifically adapted to reduce return loss;

wherein at least one of said first through fourth stages comprises a suppression circuit.

19. The filter circuit of Claim 18, wherein said fourth filter stage is disposed in electrical series between said at least one output terminal and the rest of said first, second and third filter stages within said circuit.

20. The filter circuit of Claim 19, wherein said fourth stage comprises at least one tank circuit having at least one inductive element and at least one capacitive element disposed in electrical parallel with one another.

21. The filter circuit of Claim 18, wherein said switch is actuated in response to at least DC loop current.

22. The filter circuit of Claim 21, wherein said at least DC loop current is generated in response to an off-hook transient.

23. The filter circuit of Claim 18, wherein said switch comprises a reed switch.

24. The filter circuit of Claim 18, further comprising a second switch disposed within one of said first, second or third filter stages.

25. (Cancelled)

26. The filter circuit of Claim 18, wherein said suppression circuit is disposed in electrical series with said first, second, and third filter stages.

27. The filter circuit of Claim 26, wherein said suppression circuit comprises at least one capacitor adapted to attenuate any voltage spikes that are generated due to on-hook or off-hook transients.

28. The filter circuit of Claim 18, further comprising a suppression circuit disposed within one of said first, second, and third filter stages.

29. A telecommunications filter circuit, comprising:

first and second input terminals;

first and second output terminals;

at least first and second inductors disposed in electrical series between said first input and first output terminals;

at least third and fourth inductors disposed in electrical series between said second input and second output terminals;

at least one switch inductively coupled to at least one of said first and third inductors, said switch disposed in electrical series with at least one capacitor between first and second common points, said common points being in electrical series with said first and second output terminals, respectively; and

a suppression circuit coupled between said common points and said input terminals, said suppression circuit being adapted to at least mitigate voltage transients generated through actuation of said at least one switch due to connected equipment transients from being fed back to said input terminals.

30. The filter circuit of Claim 29, further comprising fifth and sixth inductors disposed in electrical series with said first and second inductors, and third and fourth inductors, respectively, said fifth and sixth inductors being adapted to reduce return loss.

31. The filter circuit of Claim 30, wherein said fifth and sixth inductors are part of respective ones of tank circuits.

32. The filter circuit of Claim 31, wherein said at least one switch is actuated in response to at least DC loop current.

33. The filter circuit of Claim 32, wherein said at least DC loop current is generated in response to an off-hook transient.

34. The filter circuit of Claim 29, further comprising at least one second switch disposed in electrical parallel with said at least one switch and said at least one capacitor.

35. The filter circuit of Claim 29, wherein said at least first and third inductors are disposed within respective ones of tank circuits, said tank circuits being disposed in electrical series with said first and second inductors, and said third and fourth inductors, respectively.

36. A telecommunication impedance blocking filter circuit, comprising:

at least one input terminal;

at least one output terminal;

a first filter stage disposed in electrical series between said at least one input and output terminals;

a second filter stage disposed in electrical series with said first filter stage, said second stage comprising a capacitor and switch disposed in series with at least one another; and

a suppression circuit disposed in electrical series with said first and second filter stages, said suppression circuit being adapted to suppress voltage transients occurring within said filter circuit as the result of actuation of said switch during at least one of an on-hook to off-hook, or off-hook to on-hook, transient.

37. The filter circuit of Claim 36, further comprising a third filter stage having at least first and second tank circuits.

38. The filter circuit of Claim 36, wherein one of said first and second filter stages comprises at least first and second tank circuits.

39. A telecommunications circuit comprising:

first and second circuit paths disposed substantially in electrical parallel to one another between respective sets of inputs and output terminals, said first and second circuit paths each comprising a plurality of inductive elements;

a capacitor and switch disposed in series with at least one another, said capacitor and switch being disposed electrically between said first and second circuit paths; and

a suppression circuit disposed electrically between said first and second circuit paths, said suppression circuit being adapted to suppress voltage transients occurring within said filter circuit as the result of actuation of said switch during at least one of an on-hook to off-hook, or off-hook to on-hook, transient.

40. (Cancelled)

41. A telecommunication impedance blocking filter circuit, comprising:

at least one input terminal;

at least one output terminal;

a first filter stage disposed in electrical series between said at least one input and output terminals;

a second filter stage disposed in electrical series with said first filter stage, said second stage comprising a capacitor and switch disposed in series with at least one another; and

a suppression circuit disposed electrically between said at least one input terminal and said second filter stage, said suppression circuit being adapted to at least mitigate voltage transients generated through actuation of said switch from being fed back to said at least one input terminal.

42. The filter circuit of Claim 41, wherein said circuit is coupled to at least one telecommunications device via said at least one input terminal, and said mitigation of voltage transients prevents interruption of the operation of said at least one device.

43. The filter circuit of Claim 42, wherein said at least one telecommunications device comprises an ADSL modem.

44. The filter circuit of Claim 41, further comprising a tank circuit having an inductive element and capacitive element disposed in electrical parallel with one another, said tank circuit being disposed electrically between said second filter stage and said at least one output terminal.

45. The filter circuit of Claim 41, further comprising a third filter stage disposed in electrical series with said first and second filter stages, said fourth stage being adapted to reduce return loss.

46. The filter circuit of Claim 44, further comprising a third filter stage disposed in electrical series with said first and second filter stages, said fourth stage being adapted to reduce return loss.

47. A telecommunication impedance blocking filter circuit, comprising:

a plurality of input terminals;

a plurality of output terminals;

a first filter stage disposed in electrical series between said at input and output terminals;

a second filter stage disposed in electrical series with said first filter stage, said second stage comprising a capacitor and switch disposed in series with at least one another; and

a suppression circuit disposed electrically between said first and second filter stages, said suppression circuit being adapted to at least mitigate voltage transients generated through actuation of said switch due to connected equipment transients from being fed back to said input terminals in order to mitigate the effect of said transients on external equipment connected to said input terminals.

48. The filter circuit of Claim 47, further comprising a tank circuit stage having first and second tank circuits each having an inductive element and capacitive element disposed in electrical parallel with one another, said tank circuit stage being disposed electrically between said second filter stage and said output terminals.